REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

This is an appeal of claims 25 through 31, all of the rejected claims. Claims 1 through 24 and claims 32 through 37 are canceled from consideration.

STATUS OF AMENDMENTS

This appeal is from a non-final action of April 20, 2006. No amendment to the claims under appeal has been filed.

SUMMARY OF CLAIMED SUBJECT MATTER

Claims 25 and 28 are independent claims. Claims 25 describes a device that has the following elements:

a. an integrated circuit chip having a plurality of contact pads, described on page 11, the first and second paragraph, depicted as element 104 in Figure 1;

b. a single-layered insulating interposer film having a top surface and a bottom surface, described on page 9, third paragraph, depicted as element 101 in Figure 1;

c. an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating film, described on page 10, first paragraph, depicted as element 103 in Figure 1;

d. vias extending through the interposer filled with conductive material, which contact the conductive pattern and form exit ports on the bottom surface, the bottom surface immediately

adjacent the exit ports free of a conductive pattern and contact pad, described in the first and the second paragraph of page 13, depicted as element 107b in Figure 1; and

e. thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer, described in the first, second, and third paragraph of page 12, and depicted as element 106 in Figure 1.

Claim 28 describes a substrate for connecting an integrated circuit chip. The substrate has the following elements:

a. a single-layered insulating interposer film, described on page 9, third paragraph, depicted as element 101 in Figure 1;

b. an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating interposer film, described on page 10, first paragraph, depicted as element 103 in Figure 1;

c. vias extending through the interposer, filled with conductive material, contacting the conductive pattern, and forming exit ports on the bottom surface; and the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad, described in the first and the second paragraph of page 13, depicted as element 107b in Figure 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 25 through 31 are rejected under 35 U.S.C. 103(a) as obvious over Miles et al.[1] in view of Taniguchi et al.[2]

[1] US Patent No. 5,535,101, issued Jul. 9, 1996, on an application filed Nov. 3, 1992 by Miles et al.
[2] US Patent No. 5,953,592, issued Sep. 14, 1999, on an application filed Jul. 28, 1998 by Taniguchi et al.